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| Applicant: | Gajinder Singh PANESAR |
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| For: | DESIGN OF AN APPLICATION SPECIFIC PROCESSOR (ASP) |
| Examiner: | Thai Phan |
| Art Unit: | 2123 |



CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

The undersigned hereby certifies that this document is being placed in the United States mail with first-class postage attached, addressed to the Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on June 15, 2004.

Eileen MacKenzie

**Mail Stop Amendment**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

## REQUEST FOR RECONSIDERATION

In response to the Office Action mailed January 15, 2004, Applicant respectfully requests reconsideration. Claims 1-7 are pending in this application. Claims 1-5 are allowed and claims 6 and 7 are rejected. The application as presented is believed to be in condition for allowance.

As a preliminary matter, Applicant notes with appreciation the allowance of claims 1-5.

The Office Action rejected claims 6 and 7 under 35 U.S.C. §103(a) as purportedly being obvious over Aleksic (5,995,736) in view of Shrote (5,774,358). Applicant respectfully traverses this rejection, as the combination of Aleksic and Shrote is improper. Furthermore, even if Aleksic and Shrote were combined as set forth in the Office Action, Applicant's claims patentably distinguish over any such combination.

Initially, it is noted that the Office Action asserts that Shrote teaches, "converting functional model into generated instruction code for subsequent phase simulation or verification." *See* Office Action, page 3, line 20 – page 4, line 3. While Applicant disagrees that such a teaching is found in Shrote, it is Applicant's understanding that the Office Action is asserting that the limitation of claim 1 which recites, "means for converting the functional model, including its state at the end of the predetermined simulation phase, into a simulation language for simulating the ASP at circuit level," reads on this alleged teaching of Shrote. In addition, as discussed below, it is Applicant's understanding that the Office Action relies on this alleged teaching of Shrote as a basis for combining the references.

If Applicant's understanding of these assertions is inaccurate, the Examiner is respectfully requested to provide clarification with respect to these assertions.

***The Combination of Aleksic and Shrote***

One of skill in the art would not have been motivated to combine Aleksic and Shrote in the manner suggested in the Office Action. The Office Action asserts that one of skill in the art would have been motivated to modify Aleksic by incorporating into Aleksic the feature of converting the functional model, including its state at the end of the predetermined simulation phase, into a simulation language for simulating the ASP at circuit level, as purportedly taught by Shrote. *See* Office Action, page 3, line 20 – page 4, line 3 and page 5, lines 9-13. Applicant respectfully disagrees with this assertion.

The Office Action relies on the assertion that Shrote teaches converting a functional model, including its state at the end of the predetermined simulation phase, into a simulation language for simulating an ASP at circuit level as a basis for combining Aleksic and Shrote. However, there is no such teaching in Shrote. Any such teaching comes only from Applicant's specification and the use of Applicant's specification as a basis for combining references is improper. Therefore, the combination of Aleksic and Shrote is improper and should be withdrawn.

Specifically, Shrote does not teach or suggest converting a functional model into instruction code for subsequent simulation or verification, as the Office Action asserts. Instead, Shrote discloses that when verifying a hardware model using an instruction sequence, resources

may be destroyed by subsequent instructions before they are verified (Col. 13, lines 11-14). For example, a particular register may contain a certain value which should be checked to verify that the hardware model is operating correctly. However, if a subsequent instruction is a load instruction which loads a new value into that register, the previous value in that register will be overwritten (Col. 13, lines 14-22). Thus, it is necessary to verify the value of that register is correct before it is overwritten. Shrote achieves this by including instructions in the code stream that drive the register to a verifiable value and then verify the value of the register before it is overwritten (Col. 13, lines 32-37).

Shrote teaches that the code stream (i.e., instruction data stream 214) used to verify the hardware model is generated by code/data generation entity 210 (Col. 6, lines 15-19). The code/data generation entity generates the instruction data stream 214 using templates 216, such as the template shown in Example 1 of Shrote (Col. 8, lines 1-18). This code stream is not, as stated in the Office Action, generated from a functional model of the circuit that includes the state of the functional model at the end of a particular simulation phase.

As Shrote does not teach converting the functional model, including its state at the end of the predetermined simulation phase, into a simulation language for simulating the ASP at circuit level, it would not have been obvious to modify Aleksic to include this feature based on the disclosure of Shrote. Accordingly, it is respectfully requested that rejection of claims 6 and 7 under 35 U.S.C. §103(a) be withdrawn.

***Claims 6 and 7 Patentably Distinguish Over the Combination of Aleksic and Shrote***

**Claim 6**

Claim 6 is directed to a computer system for simulating an ASP comprising: first processor means including execution means for simulating a functional model in a high level language and output means for outputting the state of the functional model at the end of a predetermined simulation phase; means for converting the functional model, including its state at the end of the predetermined simulation phase, into a simulation language for simulating the ASP at circuit level; and second processor means arranged to execute the simulation language to simulate the ASP at circuit level for a subsequent simulation phase.

The Office Action concedes that Aleksic does not disclose "means for converting the functional model, including its state at the end of the predetermined simulation phase, into a simulation language for simulating the ASP at circuit level." *See* Office Action, page 3, lines 11-13. Further, as discussed above, Shrote does not disclose this limitation of claim 1, as Shrote discloses generating a code stream for verifying a hardware model of a circuit based upon templates and not a functional model of the circuit that includes its state at the end of a simulation phase.

Thus, claim 6 patentably distinguishes over Aleksic and Shrote, taken alone or in combination. Accordingly, it is respectfully requested that the rejection of claim 6 under 35 U.S.C. §103(a) be withdrawn.

**Claim 7**

Claim 7 is directed to a modelling file stored on a computer readable medium and comprising a first code portion holding a test functions file defining the communication attributes of a processor with a peripheral of an ASP to be simulated and including the state of the test function file after a predetermined simulation phase and a second code portion holding an interface functions file which defines the communication attributes of the peripheral with the processor and the functional attributes of the peripheral and including the state of the interface functions file after the predetermined simulation phase, wherein the code portions are within a circuit level simulation language and are executable by a computer in which the modelling file is loaded to simulate the ASP at circuit level for a subsequent simulation phase.

As should be clear from the discussion above, neither Aleksic nor Shrote, taken alone or in combination, discloses or suggests, "a test functions file defining the communication attributes of a processor with a peripheral of an ASP to be simulated and including the state of the test function file after a predetermined simulation phase," and "an interface functions file which defines the communication attributes of the peripheral with the processor and the functional attributes of the peripheral and including the state of the interface functions file after the predetermined simulation phase," as recited in claim 7.

Thus, claim 7 patentably distinguishes over Aleksic and Shrote, taken alone or in combination. Accordingly, it is respectfully requested that the rejection of claim 7 under 35 U.S.C. §103(a) be withdrawn.

## CONCLUSION

In view of the foregoing remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this request for reconsideration, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

Gajinder Singh PANESAR

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